In the Claims:

Please amend claims 1, 2, 13, 19, and 20 as follows:

1. (currently amended) A method for implementing deterministic based broken scan chain diagnostics using a computer test system connected to a Physical Failure Analysis system comprising the steps of:

generating a deterministic test pattern using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system; the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern;

utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in ~~a~~ the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain;

unloading each scan chain and identifying a last switching latch in each said scan chain;

repeating the generating, loading, ~~and~~ unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; ~~and~~

checking for consistent results of the identified last switching latch in each scan chain; and responsive to consistent results being identified, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a

physical defect; and

responsive to consistent results not being identified, selecting another deterministic test pattern.

2. (currently amended) A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 further includes the steps of ~~responsive to consistent results not being identified, of selecting another deterministic test pattern; and~~ repeating the testing steps a selected number of times with the selected deterministic test pattern.

3. (canceled)

4. (previously presented) A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of generating a deterministic test pattern includes the steps of using perturbations of one base deterministic test pattern from said base deterministic test pattern set generated by said Automatic Test Pattern Generation (ATPG) system.

5. (original) A method for implementing deterministic based broken scan chain diagnostics as recited in claim 4 wherein the step of using perturbations of one base deterministic test pattern includes the steps of applying said one base deterministic test pattern from the base deterministic test pattern set to an exclusive OR and multiplexing a selected perturbation matrix entry using said exclusive OR.

6. (original) A method for implementing deterministic based broken scan chain diagnostics as recited in claim 5 includes the steps of providing a perturbation matrix

with a plurality of perturbation matrix entries including selected ones of no invert, all invert, a predefined bit invert; rotate, and invert rotate.

7. (original) A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of generating a deterministic test pattern includes the steps of using a software Pseudo Random Pattern Generator (PRPG).

8. (original) A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of generating a deterministic test pattern includes the steps of using a set of deterministic test patterns resident in a memory.

9. (previously presented) A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying deterministic values of the deterministic test pattern to a selected one of scan chain inputs and primary inputs of latches within each scan chain.

10. (previously presented) A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying perturbation deterministic values of the deterministic test pattern to a selected one of scan chain inputs and primary inputs of latches within each scan chain.

11. (previously presented) A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying random data from a software Pseudo Random Pattern Generator (PRPG) to scan chain inputs and primary inputs of latches within each scan chain.

12. (original) A method for implementing deterministic based broken scan chain diagnostics as recited in claim 1 wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying output values from an exclusive OR receiving one base deterministic test pattern from a base deterministic test pattern set and a selected perturbation matrix entry.

13. (currently amended) Apparatus for implementing deterministic based broken scan chain diagnostics in a computer test system connected to a Physical Failure Analysis system comprising:

a set of deterministic test patterns; said set of deterministic test patterns being generated using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system in a computer test system; each of the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern;

a test control program utilizing all potential system functional paths and all system clocks on a device under test, loading a deterministic test pattern into each scan chain in ~~a~~ the device under test in a system mode using lateral insertion of respective

deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain; unloading each scan chain and identifying a last switching latch in each scan chain; repeating the generating, loading, ~~and~~ unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; and checking for consistent results of the identified last switching latch in each scan chain and responsive to consistent results being identified, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a physical defect; and responsive to consistent results not being identified, selecting another deterministic test pattern.

14. (canceled)

15. (previously presented) Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 13 wherein said set of deterministic test patterns includes perturbations of one base deterministic test pattern from said base deterministic test pattern set generated by said Automatic Test Pattern Generation (ATPG) system.

16. (original) Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 15 wherein said perturbations of one base deterministic test pattern is generated by applying said one base deterministic test pattern from the base deterministic test pattern set to an exclusive OR and multiplexing a selected perturbation matrix entry using said exclusive OR.

17. (original) Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 16 includes a perturbation matrix having a plurality of perturbation matrix entries including selected ones of no invert, all invert, a predefined bit invert; rotate, and invert rotate.

18. (original) Apparatus for implementing deterministic based broken scan chain diagnostics as recited in claim 13 wherein said set of deterministic test patterns includes a software Pseudo Random Pattern Generator (PRPG) for generating a deterministic test pattern.

19. (currently amended) A computer program product for implementing deterministic based broken scan chain diagnostics of a device under test in a computer test system connected to a Physical Failure Analysis system, said computer program product including instructions stored on a computer recording medium consisting one of a floppy disk, an optically read compact disk, a compact disk read only memory (CD-ROM), and a tape, wherein said instructions, when executed by the computer test system to cause the computer system to perform the steps of:

generating a deterministic test pattern using a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system; the deterministic test pattern being a predetermined Level Sensitive Scan Design (LSSD) pattern;

utilizing all potential system functional paths and all system clocks on a device under test, loading the deterministic test pattern into each scan chain in ~~a~~ the device under test in a system mode using lateral insertion of respective deterministic values of the deterministic test pattern into each of a plurality of latches of each said scan chain

via system data ports and applying system clocks to capture the respective deterministic values in each of the plurality of latches of each said scan chain;

unloading each scan chain and identifying a last switching latch in each scan chain;

repeating the generating, loading, ~~and~~ unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the deterministic test pattern; ~~and~~

checking for consistent results of the identified last switching latch in each scan chain; and responsive to consistent results being identified with the deterministic test pattern, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a physical defect; and

responsive to consistent results not being identified, selecting another deterministic test pattern.

20. (currently amended) A computer program product for implementing deterministic based broken scan chain diagnostics as recited in claim 19 includes the steps responsive to consistent results not being identified, ~~of selecting another deterministic test pattern; and~~ repeating the generating, loading, ~~and~~ unloading and identifying a last switching latch in each said scan chain testing steps a selected number of times with the selected deterministic test pattern.